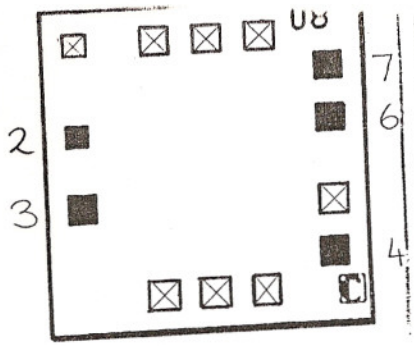
Sierra Components, Inc.

2222 Park Place Building 3 Suite E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function
1	NC
2	V_{inv}
3	$V_{non-inv}$
4	$-V_{cc}$
5	NC
6	V_{out}
7	$+V_{cc}$
8	NC

NOTE: Chip back may be connected to $-V_{cc}$ or it may be floated.

E & O E. The supply of dice to this layout can only be guaranteed if it forms part of a specification or the chip identification, where given below, is requested. Chip back potential is the level at which bulk silicon is maintained by on-chip connection, or it is the potential to which the chip back must be connected when specifically stated in a NOTE above. If no potential is given the chip back should be isolated. Nominal metallisation thicknesses are based on manufacturer's information. 1 mil. = 0.001 inch. Tolerances on dimensions +/- 3 mils.

Topside Metal:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY: **DIE SIZE (Mils): 54 X 54 X 14** **DATE: 4/19/00**
MFG: National **THICKNESS:** **P/N: CLC404ALC**